REMARKS

Claims 1-2 and 4-18 are pending. Claims 12-18 have been withdrawn from consideration pursuant to applicants' Response to Restriction Requirement of September 24, 2004. Claim 3 has been cancelled herein. Claim 1 has been amended to combine original claim 1 and original claim 3. Claims 4 and 5 have been amended in order to provide for proper antecedent basis.

Applicants' Response to the Claim objection under 37 CFR 1.75(c)

The amendment to claim 7 is to address to the claim objection under 37 CFR 1.75(c). Applicants have amended the claim to be dependent only from claim 1. Applicants respectfully submit that claim 7 is now in proper form.

Applicants' Response to the Claim Rejections under 35 U.S.C. §103

Claims 1, 2, 6, 7 and 9-11 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Hasegawa et al.* (U.S.P. 6,452,274) in view of *Matsunaga et al.* (U.S.P. 6,559,548). Claims 3-5 are rejected under 35 U.S.C. §103(a) as being unpatentable over *Hasegawa et al.* and *Matsunaga et al.* in view of *Hagiwara* (JP 2001-168093 A). Claim 8 is rejected under 35 U.S.C §103(a) as being unpatentable over *Hasegawa et al.* and *Matsunaga et al.* in view of *Shaffer, II et al.* (U.S. 2002/0052125A). In response thereto, applicants have amended the claims to more distinctly claim the subject matter regarded as the invention. Specifically, applicants have amended claim 1 to include the limitations of original claim 3. As to the rejection of original claim 3, now amended claim 1, applicants respectfully traverse as follows.

Amended claim 1 includes the features that the semiconductor device includes the first and the second dummy patterns formed near the interconnection structure, the second dummy pattern is connected to the first dummy pattern through a via portion, and the second dummy

pattern includes a plurality of discrete patterns periodically formed so as to make a pattern density substantially uniform in plane. The mechanical strength of the first and the second insulating films near the interconnection structure can be improved by connecting the first dummy pattern and the second dummy pattern to each other through the via portion. Thus, according to these features of the present invention, the first and the second insulating film can be prevented from cracking or peeling due to mechanical and/or thermal stresses at the interface between the first insulating film and second insulating film or in the first and the second insulating films.

The first and the second dummy patterns are formed for decreasing intra-plane variations of polishing amount, e.g., dishing due to overpolishing of copper or erosion due to overpolishing of the inter-layer insulating films in the CMP process for forming the interconnections by damascene process (see, e.g., page 14, lines 18 of the specification of the present application). As such, the dummy patterns have a plurality of discrete patterns periodically formed (see, e.g., FIG. 2) so as to make the pattern density of the interconnection layer substantially uniform in plane in order to achieve the prescribed object. The present invention utilizes the dummy patterns for improving the mechanical strength of the inter-layer insulating film near the interconnection structure.

Hasegawa et al. discloses in FIG. 7F the semiconductor device including the dummy interconnections 72, 82 formed near the interconnections 71, 81. The dummy interconnection 82 is connected to the dummy interconnection 72 via the dummy via contact plugs 75. In *Hasegawa et al.*, the dummy interconnections 72, 82 are formed as paths for heat dispersion to disperse the heat generated in the semiconductor device to the outside. The dummy interconnections 72, 82

are inserted at locations of interconnection spaces at least three times the minimum pitch so as to eliminate locations of interconnection spaces of more than 1 μm (see, e.g., column 15, lines 53-60). The dummy via contact plugs 75 are formed for further enhancing the heat dispersion effect (see, e.g., column 19, lines 50 – 52).

As described above, the dummy interconnections 72, 82 of *Hasegawa et al.* are formed as the paths for heat dispersion. On the other hand, the first and the second dummy patterns of the present invention per amended claim 1 are for decreasing intra-plane variations of a polishing amount in the CMP process. Thus, the dummy interconnections of *Hasegawa et al.* and the dummy patterns of amended claim 1 clearly differ with each other.

The dummy interconnections of Hasegawa *et al.* are inserted at locations of interconnection spaces at least three times the minimum pitch so as to eliminate locations of interconnection spaces of more than 1 μm. That is, the patterns of the dummy interconnections 72, 82 are closely related to the patterns of the interconnections 71, 81 and are arranged in consideration of the relationship with the patterns of the interconnections 71, 81.

On the other hand, the dummy patterns of amended claim 1 are formed so as to make a pattern density "substantially uniform in plane." That is, the plurality of discrete patterns forming the dummy patterns are periodically formed in the regions where the interconnection structures are not formed. The dummy patterns are not closely related to the patterns of the interconnection structures. The dummy patterns for decreasing intra-plane variations of a polishing amount in the CMP process as of the present invention contribute little to the paths for heat dispersion.

Thus, *Hasegawa et al.* clearly differs from the present invention, nor does it provide any motivation for the structure of the present invention as set forth in amended claim 1. One of ordinary skill in the art would not have found it obvious to connect to each other the dummy patterns for CMP via the contact plug in order to enhance the heat dispersion effect based on the disclosure of *Hasegawa et al.*

Hagiwara (JP 2001-168093 A) discloses in FIG. 1 the semiconductor device including the dummy interconnections 2, 8 connected to each other via the dummy hole 7. The dummy interconnections 2, 8 are formed for preventing the inter-layer insulating films from peeling off or cracking by the thermal stress applied to the outer peripheral part of the semiconductor chip. The thermal stress applied to the outer peripheral part of the semiconductor chip is caused by the thermal expansion coefficient difference between the passivation film formed on the semiconductor chip and the encapsulation resin for packaging the semiconductor chip. The dummy interconnections 2, 8 are formed in the chip outer peripheral regions 12 along the scribe lines 11 as shown in FIG. 2.

As described above, the dummy interconnections 2, 8 of *Hagiwara* are formed for preventing the inter-layer insulating films from peeling off or cracking by the thermal stress applied to the outer peripheral part of the semiconductor chip. Thus, the dummy interconnections 2, 8 of *Hagiwara* are formed only in the chip outer peripheral regions 12. The dummy interconnections 2, 8 are not formed in the major part of the semiconductor chip region. The dummy interconnections 2, 8 are not formed periodically and substantially uniform in plane.

On the other hand, the first and the second dummy patterns of the present invention are for decreasing intra-plane variations of a polishing amount in the CMP process. The dummy

patterns are formed so as to make a pattern density of the interconnection layers substantially uniform in plane. That is, the plurality of discrete patterns forming the dummy patterns are periodically formed in the whole semiconductor chip region. Thus, the dummy interconnections of *Hagiwara* and the dummy patterns of the present invention as set forth in amended claim 1 clearly differ from each other.

In *Hagiwara,* the dummy interconnection 8 is connected to the dummy interconnection 2 via the dummy via hole 7. However, as described above, the dummy interconnections 2, 8 are clearly differs from the dummy patterns of the presently claimed invention. Thus, the disclosure of *Hagiwara* does not provide any motivation for connecting to each other the dummy patterns for CMP via the contact plug.

As described above, *Hasegawa et al.* and *Hagiwara* clearly differ from the present invention and do not provide any motivation for the invention as claimed in amended claim 1. Applicants further submit that *Matsunaga et al.* and *Shaffer, II et al.* neither teach nor suggest the dummy interconnection pattern.

Thus, applicants respectfully submit that the present invention as set forth in amended claim 1 and all dependent claims there from, i.e. claims 2, 4-10 would not have been obvious to one of ordinary skill in the art at the time the invention was made, even in light of the combination of *Hasegawa et al., Hagiwara, Matsunaga et al.* and *Shaffer, II et al.* Applicants further respectfully submit that in light of the remarks above, claim 11 would also not be obvious to one skilled in the art.

For at least the foregoing reasons, it is believed that this application is now in condition for allowance. If, for any reason, it is believed that this application is not in condition for

allowance, Examiner is encouraged to contact the Applicants' undersigned attorney at the telephone number below to expedite the disposition of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP

Michael J. Caridi
Attorney for Applicants
Registration No.: 56,171
Telephone: (202) 822-1100
Facsimile: (202) 822-1111

MJC